Multiple	Term	Docs	Hits
☐	WALKER-ZAKIYA.XA.	266	266
☐	WALKER-ZAKIYA-N.XA.	1	1
☐	WALKE-AMANDA.XA.	2	2
☐	WALKE-AMANDA-C.XA.	219	219
☐	WALKINS.XA.	2	2
☐	WALKINS-III-WILLIAM-P.XA.	1	1
☐	WALKINS-KEVIN-M.XA.	1	1
☐	WALKONSKI.XA.	1	1
☐	WALKONSKI-JOSEPH-A.XA.	1	1
☐	WALKOWSKI.XA.	171	171
☑	WALKOWSKI-JOSEPH-A.XA.	162	162
☑	WALKOWSKI-JR-JOSEPH-A.XA.	7	7
☑	WALKOWSKI-JR-J-A.XA.	2	2
☐	WALL.XA.	6	6
☐	WALLA.XA.	2	2
☐	WALLACE.XA.	1474	1474
☐	WALLACE-AMANDA-C.XA.	1	1
☐	WALLACE-BRYAN.XA.	9	9
☐	WALLACE-BRYAN-C.XA.	6	6
☐	WALLACE-C.XA.	2	2
☐	WALLACE-CAROL.XA.	12	12

Browse Previous Page | Browse Next Page

```
"WALKOWSKI-JOSEPH-A".XA.
"WALKOWSKI-JR-JOSEPH-A".XA.
"WALKOWSKI-JR-J-A".XA.
```

Search | Clear

Help | Logout | Interrupt

Main Menu | Show S Numbers | Edit S Numbers | Preferences | Cases

John

WEST

Dictionary Search

Database:

- US Patents Full-Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Change DB

Enter a dictionary search term:

Browse

Browse Type	Max Returned Terms	Min number of documents the term appears in
○ ROOT ○ STEM ◉ EXPAND	10	

Change

WEST

Generate Collection | Print

L3: Entry 1 of 171 File: USPT Dec 21, 1976

US-PAT-NO: 3999004
DOCUMENT-IDENTIFIER: US 3999004 A
**** See image for Certificate of Correction ****

TITLE: Multilayer ceramic substrate structure

DATE-ISSUED: December 21, 1976

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chirino; Octavio I.	Endwell	NY		
Hromek; Joseph	Endwell	NY		
Joshi; Kailash C.	Endicott	NY		
Phillips, Jr.; George C.	Endwell	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 05/ 509772 [PALM]
DATE FILED: September 27, 1974

INT-CL: [02] H05K 1/04, H05K 1/14

US-CL-ISSUED: 174/68.5; 29/625, 264/61, 264/62, 264/131, 427/96, 427/97
US-CL-CURRENT: 174/257; 174/266, 264/131, 427/96, 427/97

FIELD-OF-SEARCH: 29/624, 29/625, 29/628, 174/68.5, 174/DIG.3, 317/11A, 317/11B, 317/11CE, 317/11CM, 317/11D, 117/201, 117/212, 117/213, 117/229, 117/8.5, 117/18-23, 117/31, 117/38, 117/54, 117/66, 117/101, 117/105, 117/105.4, 117/107.1, 117/119.6, 118/55, 118/56, 118/320, 118/52, 264/60-62, 264/131, 264/132, 264/134, 427/96, 427/97

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3661638	May 1972	Lemecha	117/212
☐	3699919	October 1972	Coffman	118/56
☐	3770529	November 1973	Anderson	174/68.5 X
☐	3852877	December 1974	Ahn	27/625

ART-UNIT: 321

PRIMARY-EXAMINER: Lanham; C.W.

ASSISTANT-EXAMINER: Walkowski; Joseph A.

ATTY-AGENT-FIRM: Neave; Charles S.

ABSTRACT:

This is a microelectronic multilayer circuit structure having circuit compatibility encapsulated within the circuit package including conductive electrical interconnection means formed by uniquely metallizing the "via" and/or blind interconnection holes within the circuit package. The assembly process provides means of uniformly metallizing the interlayer connecting holes.

9 Claims, 9 Drawing figures

WEST

Generate Collection Print

L3: Entry 21 of 171 File: USPT Jan 27, 1976

US-PAT-NO: 3934335
DOCUMENT-IDENTIFIER: US 3934335 A

TITLE: Multilayer printed circuit board

DATE-ISSUED: January 27, 1976

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nelson; Mark A.	Dallas	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 05/ 515282 [PALM]
DATE FILED: October 16, 1974

INT-CL: [02] H05K 3/18, H05K 3/28

US-CL-ISSUED: 29/625; 96/36.2, 174/68.5, 317/101B, 427/96
US-CL-CURRENT: 29/847; 174/266, 361/779, 361/795, 427/96, 430/311, 430/313, 430/315

FIELD-OF-SEARCH: 29/625, 96/36.2, 96/38.4, 174/68.5, 117/212, 117/213, 117/215, 117/217, 117/5.5, 117/6, 117/8.5, 117/66, 117/67, 317/11A, 317/11B

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3366519	January 1968	Pritchard et al.	156/3
☐	3525617	August 1970	Bingham	156/3 X
☐	3540954	November 1970	Pritchard et al.	156/3
☐	3622384	November 1971	Davey et al.	317/101A X
☐	3628999	December 1971	Schneble et al.	317/101B X
☐	3666549	May 1972	Rhodenizer et al.	96/36.2 X
☐	3679941	July 1972	Lacombe et al.	317/101A
☐	3698940	October 1972	Mersereau et al.	117/212
☐	3745095	July 1973	Chadwick et al.	174/68.5 UX
☐	3846166	November 1974	Saiki et al.	174/68.5 X

ART-UNIT: 321

PRIMARY-EXAMINER: Lanham; C. W.

ASSISTANT-EXAMINER: Walkowski; Joseph A.

ATTY-AGENT-FIRM: Levine; Harold Grossman; Rene E. Bandy; Alva H.

ABSTRACT:

Multilayer printed circuit board is fabricated by coating a suitable substrate, metal, plastic, paper, with a photosensitive coating, exposing the photosensitive coating to form a dielectric thereof, coating the dielectric layer with a coating of a photosensitive chemical solution, selectively imaging and developing the photosensitive coating to form a desired circuit pattern on the dielectric coating, forming a first layer of circuitry by coating the circuit pattern with a conducting material, coating the circuitry bearing layer with a second layer of photosensitive material, selectively exposing and developing the second layer of photosensitive material to form a dielectric with open windows to the first circuit layer, coating the second dielectric layer of the first circuitry with a coating of photosensitive chemical solution, selectively imaging and developing the coating of photosensitive chemical solution to form a circuit pattern and an interconnect pattern and forming a conductor layer of circuitry and interconnects, the interconnect metallization connecting the second circuitry layer with the first circuitry layer, repeating the process to form additional circuitry layers to perform a desired electrical function and forming on the last dielectric layer a metallization such as either a solder mask for circuit terminals or a ground plane and thereafter either retaining the substrate if desired for, for example, a heat sink or additional support or both, or removing the substrate to form a very light weight multilayer printed circuit board.

11 Claims, 10 Drawing figures